Green Design: Lead-Free Technologies

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Agenda

- Background — T. Brady
- Industry Challenges — M. Garner
- Technology Status — V. Gupta
- Questions & Answers

Lead-free: State of Play

EU Draft legislation requires electronics to be lead-free by 2006-2007.

Japan

Select products marketed as “lead-free.”

US

No direct legislation or market pull.

Products must be lead-free by 2006-2007

Lead – Where is it?

Monitor ~900 g (2 lbs)

Printed Circuit Board 5-10 g

Microprocessor ~0.2 g

Peripherals 2-3 g

For comparison:

- House key ~0.1-0.3 g
- Car battery = 9000 g (20 lbs)

Intel's Lead-free Position

Intel is committed to finding appropriate and cost-effective ways to reduce lead in its products. To accomplish this mission, Intel is working proactively with other companies in the industry to establish standards and identify compatible technologies to support the migration away from tin-lead solder.

Where is Intel Today?

- Intel has dedicated significant resources to lead-free R&D over the past 2 years
- Intel has developed lead-free solutions for select package technologies
- Intel will continue to develop lead-free technologies

The time to prepare for lead-free is now!

Agenda

- Background
- ➢Industry Challenges — M. Garner
- Technology Status
- Questions & Answers

Industry Challenges

- Five key challenges
  - Material and process development
  - Backward compatibility
  - Supply chain readiness
  - Cost
  - Industry standards and conversion roadmap

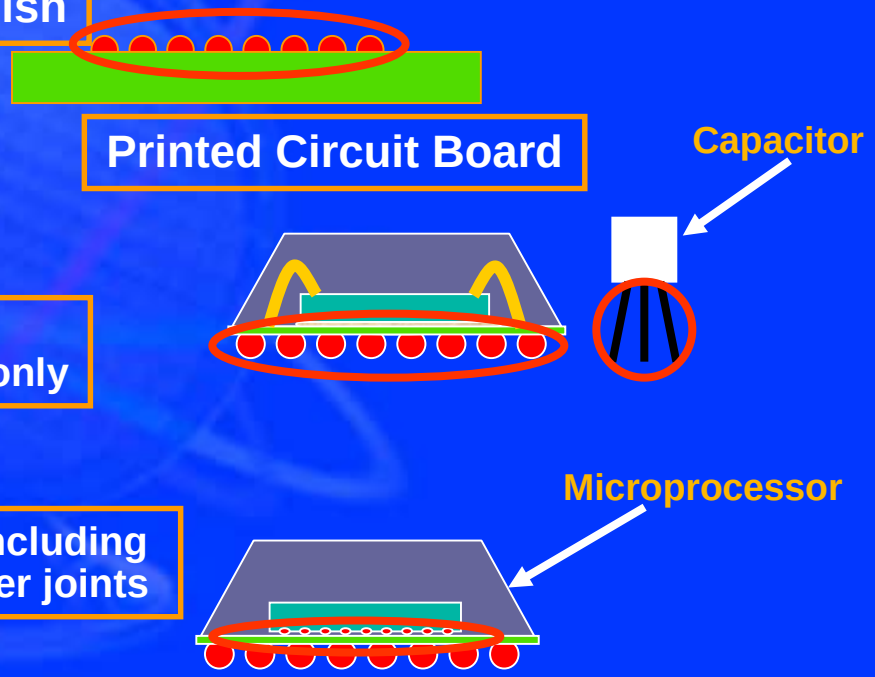
Intel Developer Forum Spring 2002

Matls & Proc: Where is lead used?

Level 3 — Pb = **Solder Paste /Board Finish**

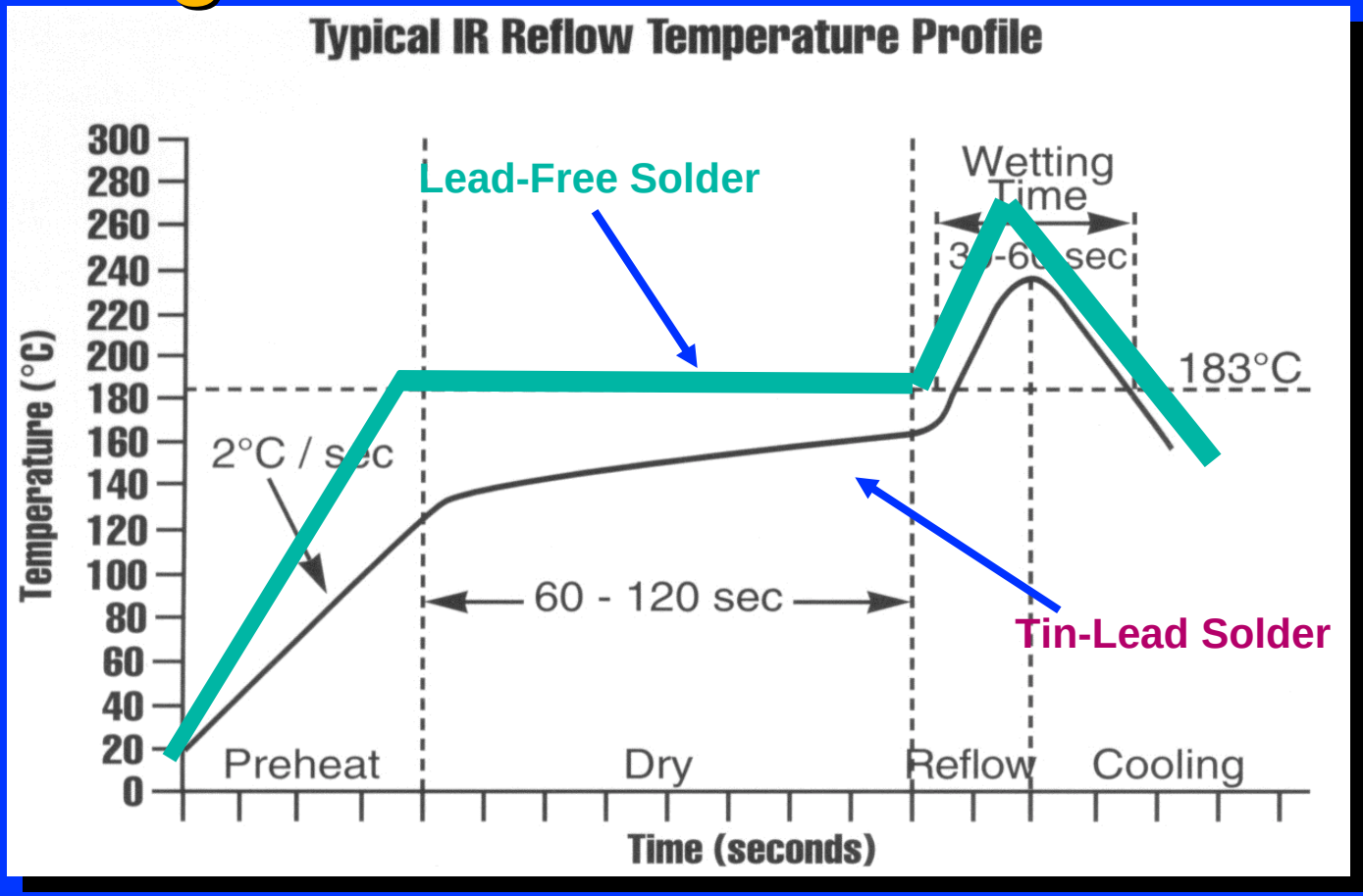
Level 2 — Pb = **IC Package Terminals only**

Level 1 — Pb = **IC Package including internal solder joints**

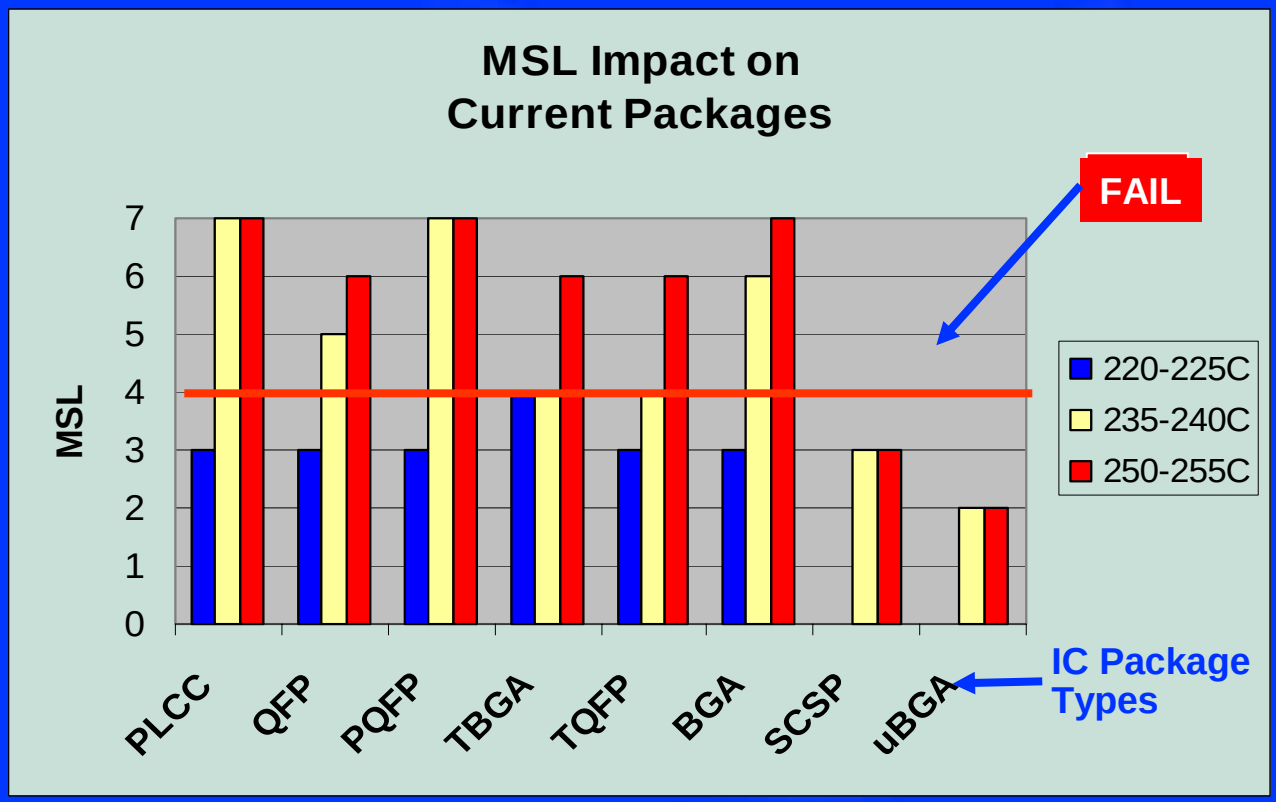


Products currently marketed as "lead-free" are typically only level 3

Matls & Proc: Higher Temp Soldering



Matls & Proc: Package Reliability



Many existing IC components cannot withstand higher processing temperatures required by lead-free solders. Materials changes are being made to meet lead-free process temperatures.

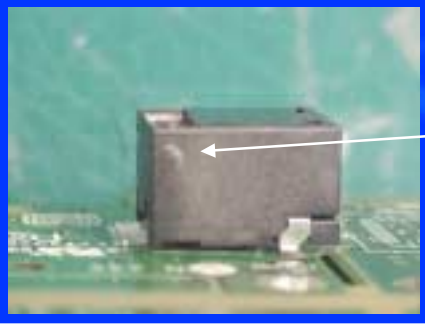
MSL = Moisture Sensitivity Level

Source: Intel Internal Data

Matls & Proc: Pb-free Temperature Compatibility Issue

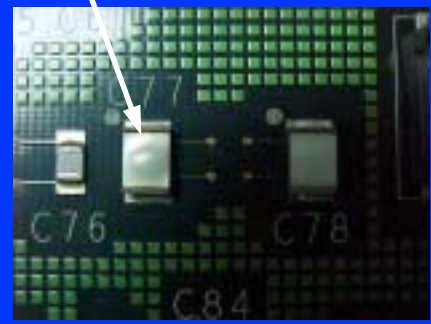
2512 Resistor lead free solder joint failures

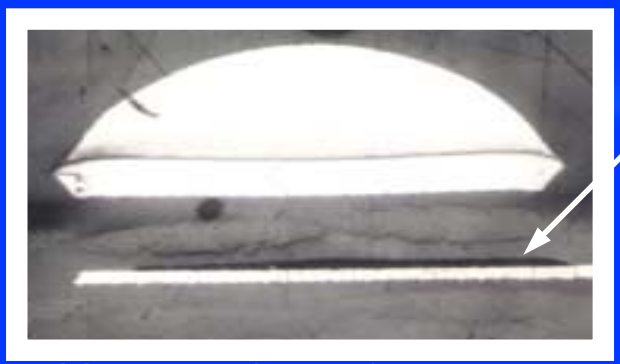
Cracked Transformer



Connector blistered on 2nd reflow

Blistered Film Capacitor





PCB delamination

Backward Compatibility

- Backward Compatibility: lead-free parts assembled using tin-lead process
  - Boards currently assembled at 210-230C
  - Lead-free solder (Sn/Ag/Cu) doesn't melt until ~220C
- During transition to lead-free there will be mixed components (lead and lead-free) on products.
- Board reliability must be validated

Supply Chain Readiness

- Key challenges for the supply chain
  - Massive number of components
  - Compatibility with higher lead-free solder temperatures
  - Lead-free solder on components
  - Board assemblers prepared
  - Industry standards for assembly

Engage with your supply chain to ensure an orderly transition to lead-free.

Cost Drivers

- Lead-free solder
- Higher temperature board assembly
- Higher temperature components

Intel development experience suggests:
- **Proactive engineering will reduce the cost impact**
- **Materials cost adders will be reduced with high volume**

Industry Conversion

- Viable transition plan needs to emerge
- Intel working with consortia to develop industry-wide solutions.
- Communicate your lead-free plans and requirements to Intel Products Groups

Join Intel and Industry Consortia to enable lead-free solutions

Agenda

- Background
- Industry Challenges
- ➢Technology Status V. Gupta
- Questions & Answers

Technology Status

- Intel has proven the feasibility of select lead-free technologies
  - Solder selection
  - Package technologies
  - PCB technology

Manufacturability of these processes must be assessed.

Solder system choice

- Solder Paste: SnAgCu
- Solder Spheres: SnAgCu
- Lead Finish: Matte Sn is the front runner.
  - Pending definition of Sn-whisker testing by NEMI task force
- Board Finish: Im Ag. OSP may be used in certain applications

Intel intends to use industry standard solutions

Lead Elimination on BGA packages

Today's Lead-Tin Process

New Lead-Free Process

Gold wire bond

Gold wire bond

Lead-Tin solder ball

Tin-Silver-Copper solder ball

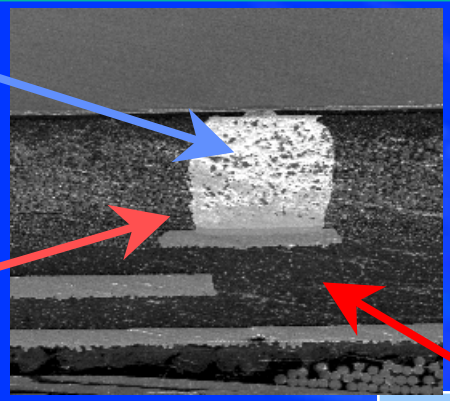
Lead Elimination on Flip Chip Packages

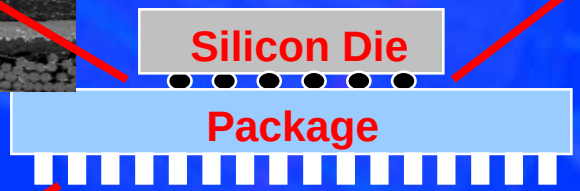
Today's Lead-Tin Process

New Lead-Free Process

Lead Bump

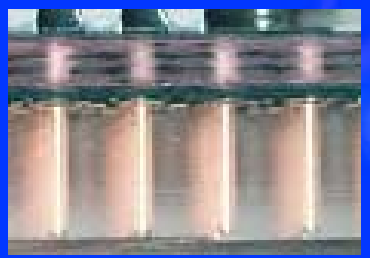
Lead-tin Solder





Evaluating technology options

Tin-Antimony Solder



Tin-Antimony Solder

Package Technology Status

- Intel has made significant progress in development of two Pb-free BGA package families
  - IPC MSL3 at 260C (1K cycles TC ”B”)
  - 1K cycles THB (85/85) w/ level 3 preconditioning and unbiased HAST (121C and 98% RH)
  - Solder joint reliability
    - 800 cycles TC “B,” 1K hrs bake @140C
    - Drop test and bend test

Yield and reliability ≥ Sn-Pb process
Pb-free materials available from suppliers

PCB Technology Status

- Pb-free assembly feasibility demonstrated
  - Solder joints reliable after 1K TC “X”
  - Reflow temperature at 245C - 250C
  - Equivalent (to Sn-Pb) assembly yield projected
- About 60% of BOM available from suppliers
  - Some components need material development
- First (small) board process development planned to be complete in 1H’02
  - Large board technology development is to start in late ‘02

Consortia Engagement

- Intel is actively engaged with key industry consortia to develop technology solutions
  - NEMI, HDPUG, JEDEC, IPC, GECI, JEITA etc.
- Several significant issues need resolution
  - Compatible solder system (GECI)
  - Assembly process parameters guideline (NEMI/ HDPUG)
  - Supply chain readiness (GECI)
  - Industry conversion roadmap (GECI)

Get involved and make sure that your needs are addressed.

Summary

- The time to prepare for lead-free technologies is now
- Development of lead-free technologies is underway at Intel
- Significant technical & logistic challenges remain

Join Intel and Industry Consortia to develop a viable industry transition plan

Questions?

Collateral

- Intel Pb-free program update can be found at:

http://www.intel.com/research/silicon/leadfree.htm

- Contact Names
  - For specific lead-free product availability see your Intel Sales team.

Acronyms

- GECI - Global Environmental Coordination Initiative
- HDPUG - High Density Package User Group
- JEITA - Japan Electronics and Information Technologies Industries Alliance
- NEMI - National Electronics Manufacturing Initiative
- MRC – Management Review Committee
- SC – Steering Committee

Intel Lead-Free Package Technology

- Todd Brady, Mike Garner, Vivek Gupta
- Intel Corporation

Please remember to turn in your session survey form